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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,700	12/13/2004	Manfred Kirschner	3151	8611

7590 09/28/2006

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EXAMINER	
WASHBURN, DOUGLAS N	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/517,700	KIRSCHNER ET AL.	
	Examiner	Art Unit	
	Douglas N. Washburn	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 11-14* is/are rejected.

7)☒ Claim(s) *6-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1 Applicant amendment overcomes objection to the abstract and the objection is withdrawn.

Applicant amendment overcomes §112-2 rejection of claim 13 and the rejection is withdrawn.

Applicant amendment overcomes objection to claim 13 and the objection is withdrawn.

Claim Rejections - 35 USC § 101

2 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 12 and 14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to **non-statutory subject matter**.

Claim 12 recites, "A **program code** for an electronic circuit for detecting measured values, wherein the program code is suitable for carrying out the method as recited in claim 11 when it is executed by a computing unit";

Claim 14 recites, "a **program code** as recited in claim 12, wherein the computing unit is a microcontroller in a control unit"

See MPEP 2106 V B (1) (b). Examiner further suggests http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm

.*Claim Rejections - 35 USC § 102*

3 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kerth et al. (US 5,172,115) (Hereafter referred to as Kerth).

Kerth teaches:

At least one sensor unit (110) (transducer; column 3, line 29) for generating an analog measurement signal (analog input; column 3, line 38), which represents a measured quantity (applied force or temperature; column 3, line 32) detected by the sensor unit in regard to claim 1;

A signal detecting unit (120) (ratiometric converter; column 4, line 20; figure 2) with a first analog/digital converter (121) (A/D converter; column 4, lines 25 and 26; figure 2, element 36) for digitizing the analog measurement signal (column 4, line 33 and 34) in regard to claim 1;

A voltage supply unit (130) (V_{REFi}; column 4, line 55; figure 2, element V_{REFi}) that has a first voltage source (132) (V_{REF}; column 4, line 55; figure 2, element V_{REFi}) for producing a **first supply voltage** (VS1) (**V_{REFi}**; column 4, line 55; figure 2, element V_{REFi}) with an **imprecision** x1 (**V_{OFF1}**; column 4, lines 45 and 46; figure 2, element 22) for the sensor unit (110) and has a second voltage source (134) (V_{REF}; column 4, line 53; figure 2, element V_{REF}) for producing a **second supply voltage** (VS2) (**V_{REF}**; column 4, line 53; figure 2, element V_{REF}) with an **imprecision** x2 (**V_{OFF2}**; column 4, lines 23 and 24; figure 2, element 24) for the signal detecting unit (120), the imprecisions x1 (V_{OFF1}; column 4, lines 45 and 46; figure 2, element 22), x2 (V_{OFF2}; column 4, lines 23 and 24; figure 2, element 24) being transmitted to the measurement signal, wherein the signal detecting unit (120) (ratiometric converter; column 4, line 20; figure 2) has a correction unit (127) (column 4, lines 58-64; figure 2, elements 36, 38, 48 and 50) that compensates for the effects of the imprecisions x1 (V_{OFF1}; column 4, lines 45 and 46; figure 2, element 22) and/or x2 (V_{OFF2}; column 4, lines 23 and 24; figure 2, element 24) on the digitized measurement signal in response to a **digitized voltage signal** (U) (**D_{VREF}**; column 4, lines 58 and 59; figure 2, element DV_{REF}) representing the imprecision x1 (V_{OFF1}; column 4, lines 45 and 46; figure 2, element 22) of the first supply voltage, and emits a **compensated digitized measurement signal** (M) (**D_{OUT}**; column 5, lines 24 and 25; figure 2, element D_{OUT}) resulting from the compensation in regard to claim 1;

A first memory element (127a) (offset register 80; column 6, line 42; figure 3, element 80) for storing output values of the first analog/digital converter (121) (A/D converter; column 4, lines 25 and 26; figure 2, element 36) in regard to claim 2;

A second memory element (127b) (offset register 86; column 6, line 48; figure 3, element 86) for storing values of the digitized voltage signal (U) (D_{VREF}; column 4, lines 58 and 59; figure 2, element DV_{REF}) in regard to claim 2;

A normalization unit (127d) (calibration control blocks; column 6, lines 51 and 52; figure 3, elements 82 and 88) for generating a normalization factor (N) (γ_{CALG}; column 5, line 19; figure 4, element γ_{CALG}), which is derived from the contents of the two memory elements (127a, 127b) and represents a complement to the imprecisions x1 and/or x2 in regard to claim 2;

A multiplying unit (127c) (multiplication block; column 5, lines 16 and 17; figure 4, element 60) for generating the compensated digitized measurement signal (M) (D_{OUT}; column 5, lines 24 and 25; figure 2, element D_{OUT}) by multiplying the contents of the first memory element (127a) (offset register 80; column 6, line 42; figure 3, element 80) by the normalization factor N (γ_{CALG}; column 5, line 19; figure 4, element γ_{CALG}), with a delay element (127e) that delays the supplying of the content of the first memory element to the multiplying unit (127c) (multiplication block; column 5, lines 16 and 17; figure 4, element 60) by the amount of time (calibration cycle; column 6, lines 52 and 53) that it takes to calculate the normalization factor N (γ_{CALG}; column 5, line 19; figure 4, element γ_{CALG}) in regard to claim 2;

The normalization unit (127d) (calibration control blocks; column 6, lines 51 and 52; figure 3, elements 82 and 88) calculates the normalization factor N (γ_{CALG}; column 5, line 19; figure 4, element γ_{CALG}) as follows: N = content of the first memory element/content of the second memory element (column 6, lines 51-59) in regard to claim 3;

If the first supply voltage (VS1) (V_{REFi}; column 4, line 55; figure 2, element V_{REFi}) is greater than the second supply voltage (VS2) (V_{REF}; column 4, line 53; figure 2, element V_{REF}) is characterized by:

A first voltage divider circuit (R1, R2) (ratiometric operation block; column 5, lines 9 and 10; figure 2, element 52) for generating the voltage signal (U) (D_{VREF} ; column 4, lines 58 and 59; figure 2, element D_{VREF}), which represents the imprecision x1 (V_{OFF1}; column 4, lines 45 and 46; figure 2, element 22) of the first supply voltage (VS1) (V_{REFi}; column 4, line 55; figure 2, element V_{REFi}), through division of the first supply voltage (VS1) (V_{REFi}; column 4, line 55; figure 2, element V_{REFi}), preferably in a ratio such that the voltage signal (U) (D_{VREF}; column 4, lines 58 and 59; figure 2, element D_{VREF}) corresponds quantitatively to the second supply voltage (VS2) (V_{REF}; column 4, line 53; figure 2, element V_{REF}) in regard to claim 4;

A second analog/digital converter (122) (A/D converter; column 4, lines 25 and 26; figure 2, element 38) that is operated with the second supply voltage (VS2) (V_{REF}; column 4, line 53; figure 2, element V_{REF}) and is for digitizing the voltage signal (U) (D_{VREF}; column 4, lines 58 and 59; figure 2, element D_{VREF}), the second analog/digital converter (122) (A/D converter; column 4, lines 25 and 26; figure 2, element 38) being preferably associated with the signal detecting unit (120) in regard to claim 4;

A second signal detecting unit (120') that is operated with the first supply voltage (VS1) (V_{REFi}; column 4, line 55; figure 2, element V_{REFi}) and includes a third analog/digital converter (122') that digitizes the second supply voltage (VS2) (V_{REF}; column 4, line 53; figure 2, element V_{REF}) to generate the voltage signal (U) (D_{VREF}; column 4, lines 58 and 59; figure 2, element D_{VREF}), which represents the imprecision x1 of the first supply voltage (VS1) (V_{REFi}; column 4, line 55; figure 2, element V_{REFi}), the third analog/digital converter (122') likewise being operated with the first supply voltage (VS1) (V_{REFi}; column 4, line 55; figure 2, element V_{REFi}) in regard to claim 5;

A method for operating an electronic circuit for detecting measured values as recited in claim 1 (ratiometric converter; column 4, line 20; figure 2), in particular for operating its correction unit (column 4, lines 58-64;
figure 2, elements 36, 38, 48 and 50) to compensate for imprecisions x1 (V_{OFF1}; column 4, lines 45 and 46; figure 2, element 22) and/or x2 (V_{OFF2}; column 4, lines 23 and 24; figure 2, element 24) in a digitized measurement signal in regard to claim 11;

Storage of a value of the digitized measurement signal (M) (D_{OUT}; column 5, lines 24 and 25; figure 2, element D_{OUT}) at time n in regard to claim 11;

Storage of a value at time n (calibration cycle; column 6, lines 52 and 53) of a voltage signal (U) (D_{VREF}; column 4, lines 58 and 59; figure 2, element D_{VREF}) that represents the imprecision x1 (V_{OFF1}; column 4, lines 45 and 46; figure 2, element 22) of a first supply voltage (VS1) (V_{REFi}; column 4, line 55; figure 2, element V_{REFi}) in regard to claim 11;

Calculation of a normalization factor N (γ_{CALG}; column 5, line 19; figure 4, element γ_{CALG}) by dividing the value of the digitized measurement signal at time n (calibration cycle; column 6, lines 52 and 53) by the value of the voltage signal (U) (D_{VREF}; column 4, lines 58 and 59; figure 2, element D_{VREF}) at time n (calibration cycle; column 6, lines 52 and 53) in regard to claim 11;

Generation of a compensated digital measurement signal (M) (D_{OUT}; column 5, lines 24 and 25; figure 2, element D_{OUT}) by multiplying the normalization factor N (γ_{CALG}; column 5, line 19; figure 4, element γ_{CALG}) by the value of the digitized measurement signal at time n (calibration cycle; column 6, lines 52 and 53) in regard to claim 11;

A computer program (algorithm; column 5, line 5) for an electronic circuit for detecting measured values, characterized by a program code, which is suitable for carrying out the method as recited in claim 11 when it is executed by a computing unit, in particular a microcontroller (controller; column 11, line 12) in a control unit in regard to claim 12; (for purpose of examination examiner interprets a program code as a computer program stored on computer readable medium)

The program code is stored on a data medium that is readable by a computer (register; column 5, line 14; figure 2, element 58) in regard to claim 13;
(for purpose of examination examiner interprets a program code as a computer program stored on computer readable medium)

And a program code as recited in claim 12, wherein the computing unit is a microcontroller in a control unit (system calibration unit; figure 3, element 32) in regard to claim 14. (for purpose of examination examiner interprets a program code as a computer program stored on computer readable medium)

Allowable Subject Matter

4 Claims 6-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for indicating allowable subject matter for claims 6-10 were presented in office action mailed 6 July 2006.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5 Applicant's arguments filed 8 September 2006 have been fully considered but they are not persuasive.

Applicant argues "Kerth shows a ratiometric converter, in which the input voltage is compared with an internal reference." "The supply voltage of the charged (Fig. 3, charge cell 10) and the supply voltage of the ratiometric converter are generally not considered."

"In contrast, the present invention relates to a compensation device of two supply voltages and their deviations."

Examiner notes Kerth teaches, "The system first determines in the digital domain the non-ratiometric offset values and stores these in a register and then subtracts these offset values, resulting in elimination of the non-ratiometric offsets. In one mode, each word is passed through the system to determine the non-ratiometric offset and then the non-ratiometric offset value generated and subtracted during a second pass such that each word requires two passes. In a second mode, the system is calibrated to determine the non-ratiometric offset value, and this is stored in a register. Subsequent passes through the system are utilized with a subtraction operation resulting in removal of the non-ratiometric offsets. Thereafter, the system is calibrated to remove ratiometric errors." (column 9, lines 1-15).

Further, kerth teaches, "The V_{REF} inputs of the A/D converters 36 and 38 are both connected to an internal reference voltage V_{REFI}, which is different than the reference voltage connected to line 16." (col 4, l 53-57).

Clearly, Kerth teaches two supply voltages (V_{REF} and V_{REFI}), their respective deviations (V_{OFF1}, V_{OFF2}) and their respective compensations (D_{VREF}, D_{AIN}). Therefore, Kerth reads on the broad claimed limitations and the §102(b) rejection is maintained.

Conclusion

6 Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas N. Washburn whose telephone number is (571) 272-2284. The examiner can normally be reached on Monday through Thursday 6:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DNW

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